APPLICATION NOTE

RELEASED 4/5/18

Fault Propagation Tolerance UT54LVDS, UT200SpW, 3.3V

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number
3.3V Quad Driver	UT54LVDS031LV/E	5962-98651	02, 03, 04, 05	WD03, WD07, WD28, WD30
3.3V Quad Receiver	UT54LVDS032LV/E	5962-98652	02, 03, 04, 05	WD04, WD08, WD29, WD31
3.3V Quad Receiver With Termination	UT54LVDS032LVT	5962-04201	01, 02	WD06, WD10
3.3V Serializer	UT54LVDS217	5962-01534	01, 02	WD11, WD13
3.3V Deserializer	UT54LVDS218	5962-01535	01, 02	WD12, WD14
4-Port Spacewire Router	UT200SpW4RTR	5962-08244	01	WD41
SpaceWire Physical Layer Transceiver	UT200SpWPHY01	5962-06232	01, 02	WD36

1.0 Overview

Following customer-specific reliability analysis requests, CAES Semiconductor Solutions has conducted a quantitative design analysis of the UT54LVDS and UT200SpW 3.3V products to determine the fault propagation properties of these devices. The fault propagation analysis involved design simulations to determine the potential adverse effects on the expected product 15-year life reliability, resulting from permanent exposure of the LVDS IO pins, to increased voltage and short circuit fault conditions, potentially arising from third-party products and systems interfacing with the aforementioned devices.

2.0 LVDS IO Fault Condition Functional Description

The design simulation and analysis was performed for a normal operating and cold-spare condition with a combination of operating power supply voltages (VDD) in the nominal range of 3.3V +/–0.3V and LVDS IO common mode voltages (VCM) of 3.9V, 4.0V and 4.3V all significantly above the nominal operating range, but below the absolute maximum ratings specification. Additionally, design simulations were performed for the cases of VDD=VCM=4.3V (LVDS IOs shorted to increased VDD) and VCM=VSS=0.0v (LVDS IOs shorted to ground), to determine the worst case LVDS IO current and device power dissipation in the event of this type of fault conditions. All design simulations, assumed a worst-case operating junction temperature T_J of 125°C.

2.1 Device Reliability Analysis Description

The design simulation results obtained with the fault conditions described in section 2 were used to perform a device reliability analysis, to determine the impact of the permanent application of the described fault conditions, on the expected 15-year device reliability. The reliability analysis assumed a device mounted board temperature of 85°C as worst-case application environment condition.

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3.0 Fault Tolerance Simulations and Device Reliability Analysis Results

Table 2 summarizes the design simulation and the reliability analysis results for the fault conditions determined to be worst-case based on the design simulation results obtained with the analysis described in section 2. As seen in the table, the design simulation results indicate no risk of device catastrophic runaway failure and fault propagation to the interfacing devices or systems. The only possible failure modes observed through the simulation and the analysis are electromigration for the case of the stressed LVDS outputs and Single Event Gate Rupture (SEGR) for both the stressed LVDS inputs and outputs on the UT54LVDS and UT200SpW 3.3V devices, with Time To Failure (TTF) of 0.28 years for electromigration failure mode (defined as 20% increase in contact resistance) and Mean Time To Failure (MTTF) of 166 years for SEGR failure mode, respectively.

Table 2: Fault Propagation and Reliability Analysis Results

Circuit Under Test	LVDS I/O Fault Voltage	Device Power Supply	Device Operating Mode	Board Temp.	Possible Failure Mode	Failure Propagation Hazard
LVDS Output Drivers	4.3V	3.6V	Enabled	85°C	Electromigration $TTF_{0.013\%}$ (ΔR=20%)=0.28yr	None - fails open
	4.3V	0V	Cold-spared	85°C	None	None
LVDS Input Receivers	4.3V	3.6V	Enabled	85°C	None	None
	4.3V	0V	Cold-spared	85°C	None	None
LVDS Inputs/ Outputs	4.3V (0V)	0V (3.6V)	Cold-spared or Enabled	–55°C - +125°C	SEGR MTTF=166yrs (Adams 90%)	None

In addition to the fault propagation results presented in table 2, the reliability analysis determined that if the VCM overstress condition on the LVDS outputs is eliminated and the device is brought back to operating conditions within the specified range before the TTF time has been reached, then the 15-year device reliability will not be compromised.

4.0 Summary and Conclusions

Based on the available results obtained from the design simulation and reliability analysis, we reach the following conclusions:

- UT54LVDS and UT200SpW 3.3V products, fully comply with their respective product specific SMDs. Per datasheets and SMDs, operating at the absolute maximum voltage for any extended period of time may degrade the operation and reliability of the device.
- The LVDS receiver circuits will tolerate fault condition voltages in the range –0.3V to +4.3V at the LVDS inputs without permanent damage or fault condition propagation to the device outputs in power-on or cold spare states.
- The LVDS transmitter circuits will tolerate fault condition voltages at the LVDS output in the range –0.3V to +4.3V relative to device ground reference without fault propagation in power-on or cold spare states. A reliability analysis has been carried out for overstressed LVDS outputs that concludes the LVDS driver can tolerate being overstressed at 4.3V for 0.28 year with T_{BOARD}=85°C, without compromising 15 year lifetime for VDD=3.6V. Permanently overstressed LVDS outputs will eventually fail for open circuit. The LVDS outputs can tolerate being shorted to ground indefinitely.

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Appendix A – "Reliability Analysis Detailed Results" provides a detailed summary of reliability analysis test conditions and results.

Appendix A – Reliability Analysis Detailed Results

Test Conditions #1: VCM=3.9V, VDD=3.6V, T_J =102°C (based on simulated device power dissipation and board temperature of 85°C),100% duty cycle (continuous device operation): Predicted electromigration TTF (ΔR=20%) = 0.32 years

											TTF (overstress conditions)			
layer	W_{WC} (μm)	T_B (°C)	θ_{CB} (°C/W)	θ_{JC} (°C/W)	I/O (V)	supply (V)	I_{MAX} (mA)	P_D (W)	T_J (°C)	J_{MAX} (mA/μm)	$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
M1	4.5	85	61	10	3.90	3.60	14.67	0.2382	101.91	3.2600	82.83	24.95	2.03	1.03
M2	4.5	85	61	10	3.90	3.60	14.67	0.2382	101.91	3.2600	59.83	18.02	1.47	0.75
layer	# vias (WC)	T_B (°C)	θ_{CB} (°C/W)	θ_{JC} (°C/W)	I/O (V)	supply (V)	I_{MAX} (mA)	P_D (W)	T_J (°C)	J_{MAX} (mA/μm)	$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
VIA1	15	85	61	10	3.90	3.60	14.67	0.2382	101.91	0.9780	9.45	7.74	5.09	4.55

TTF (overstress) after 15yrs @ 3.63V/T_J			
$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
82.40	24.53	1.60	0.61
59.40	17.60	1.04	0.32
$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
8.69	6.98	4.33	3.79

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Test Conditions #2: VCM=4.0V, VDD=3.6V, TJ =102°C, 100% duty cycle: Predicted electromigration TTF (ΔR=20%) =0.31 years

											TTF (overstress conditions)			
layer	W_{WC} (μm)	T_B (°C)	θ_{CB} (°C/W)	θ_{JC} (°C/W)	I/O (V)	supply (V)	I_{MAX} (mA)	P_D (W)	T_J (°C)	J_{MAX} (mA/μm)	$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
M1	4.5	85	61	10	4.00	3.60	14.68	0.2442	102.34	3.2622	81.70	24.61	2.00	1.02
M2	4.5	85	61	10	4.00	3.60	14.68	0.2442	102.34	3.2622	59.01	17.78	1.45	0.74
layer	# vias (WC)	T_B (°C)	θ_{CB} (°C/W)	θ_{JC} (°C/W)	I/O (V)	supply (V)	I_{MAX} (mA)	P_D (W)	T_J (°C)	J_{MAX} (mA/μm)	$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
VIA1	15	85	61	10	4.00	3.60	14.68	0.2442	102.34	0.97867	9.32	7.63	5.02	4.49

TTF (overstress) after 15yrs @ 3.63V/T_J			
$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
81.28	24.19	1.58	0.59
58.58	17.35	1.02	0.31
$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
8.56	6.87	4.26	3.73

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Test Conditions #3: VCM=4.3V, VDD=3.6V, T_J =104°C, 100% duty cycle: Predicted electromigration TTF (ΔR=20%) = 0.28 years

											TTF (overstress conditions)			
layer	W_{WC} (μm)	T_B (°C)	θ_{CB} (°C/W)	θ_{JC} (°C/W)	I/O (V)	supply (V)	I_{MAX} (mA)	P_D (W)	T_J (°C)	J_{MAX} (mA/μm)	$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
M1	4.5	85	61	10	4.30	3.60	14.71	0.2623	103.63	3.2692	78.40	23.62	1.92	0.98
M2	4.5	85	61	10	4.30	3.60	14.71	0.2623	103.63	3.2692	56.63	17.06	1.39	0.71
layer	# vias (WC)	T_B (°C)	θ_{CB} (°C/W)	θ_{JC} (°C/W)	I/O (V)	supply (V)	I_{MAX} (mA)	P_D (W)	T_J (°C)	J_{MAX} (mA/μm)	$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
VIA1	15	85	61	10	4.30	3.60	14.71	0.2623	103.63	0.9808	8.94	7.32	4.82	4.31

TTF (overstress) after 15yrs @ 3.63V/T_J			
$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
77.98	23.19	1.50	0.55
56.20	16.64	0.96	0.28
$TTF_{50\%}$ (yrs)	$TTF_{15.87\%}$ (yrs)	$TTF_{0.1\%}$ (yrs)	$TTF_{0.013\%}$ (yrs)
8.19	6.57	4.06	3.55

Revision History

Date	Rev. #	Author	Change Description
01/23/2018	1.0.0	SZ	Initial Release
04/05/2018	1.0.1	SZ	Updated Table 1: Cross reference of applicable products